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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,853	02/25/2004	John A. Hayden	A0312.7520US00	3634

23628 7590 09/01/2006

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EXAMINER	
SORRELL, ERON J	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,853	HAYDEN ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/25/04* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,7,8,10,11,12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heath et al. (U.S. Patent No. 4,901,234 hereinafter "Heath") in view of Bowes et al. (U.S. Patent No. 5,655,151 hereinafter "Bowes").

3. Referring to apparatus claim 1, method claim 7, Heath teaches a DMA controller comprising:

a plurality of DMA channels (see lines 47-55 of column 3); and

a prioritizer (see "arbitration control circuit 11" in figure 1) configured to map DMA requests from different DMA requesters to the DMA channels in response to programmable mapping information (see paragraph bridging columns 5 and 6, note Heath discloses that the channel assignment register and

priority assignment register are programmable either through the BIOS or via an application program).

Heath does not disclose the specific structure of the plurality of channels, therefore fails to teach each channel including a datapath for transferring data from a DMA source to DMA destination and channel control logic for controlling data transfer in response to DMA parameters.

Bowes teaches, in an analogous apparatus and method, a DMA controller (item 218 in figure 2A) with a plurality of channels (item 244 in figure 2B) each channel including a datapath for transferring data from a DMA source to DMA destination and channel control logic for controlling data transfer in response to DMA parameters (see figure 3, wherein the structure of a single channel is illustrated, and lines 37-41 of column 5, note the series of bus inputs and outputs is being construed as the "datapath" and the read and write control blocks collectively are being construed as the "control logic").

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Heath with the above teachings of Bowes. One of ordinary skill would have been motivated to make such modification in order to program additional DMA transfers before the currently active transfer has been completed increasing

system efficiency as suggested by Bowes (see lines 13-25 of column 3).

4. Referring to claim 8, Heath discloses mapping DMA grants from the DMA channels to the respective DMA requesters (see paragraph bridging columns 5 and 6).

5. Referring to claim 10, Heath discloses resolving conflicts so that each of the DMA requests is mapped to only one of the DMA channels (see paragraph bridging columns 5 and 6, note while Heath does not use the exact language of "resolving conflicts," the arbitration system disclosed ensures that the requests are mapped to the channels on a one-to-one basis, thus resolving any conflicts).

6. Referring to apparatus claims 11, and system claim 15, Heath discloses mapping DMA requests and mapping DMA grants is responsive to programmable mapping information associated with each channel (see paragraph bridging columns 5 and 6, note Heath discloses that the channel assignment register and priority assignment register are programmable either through the BIOS or via an application program).

Referring to claim 12, Heath discloses a DMA controller comprising:

a plurality of DMA channels (see lines 47-55 of column 3);

a first prioritizer configured to arbitrate among DMA requests in accordance with a predetermined assignment of priorities (see paragraph bridging columns 5 and 6, note the system of Heath initially determines if the requesting device is of a first fixed priority, wherein the requesting device has a dedicated DMA channel); and

a second prioritizer configured to map DMA requests from different DMA requesters to the DMA channels in response to programmable mapping information (see paragraph bridging columns 5 and 6, note after the initial determination is made as discussed above, a second determination is made to determine if the request is of a second programmable priority in which the requesting device is assigned to one of the programmable channels).

Heath does not disclose the specific structure of the plurality of channels, therefore fails to teach each channel including a datapath for transferring data from a DMA source to DMA destination and channel control logic for controlling data transfer in response to DMA parameters.

Bowes teaches, in an analogous apparatus, a DMA controller (item 218 in figure 2A) with a plurality of channels (item 244 in figure 2B) each channel including a datapath for transferring data from a DMA source to DMA destination and channel control logic for controlling data transfer in response to DMA parameters (see figure 3, wherein the structure of a single channel is illustrated, and lines 37-41 of column 5, note the series of bus inputs and outputs is being construed as the "datapath" and the read and write control blocks collectively are being construed as the "control logic").

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Heath with the above teachings of Bowes. One of ordinary skill would have been motivated to make such modification in order to program additional DMA transfers before the currently active transfer has been completed increasing system efficiency as suggested by Bowes (see lines 13-25 of column 3).

7. Referring to claim 15, Heath teaches a DMA controller, wherein the second prioritizer is configured to map DMA grants to respective DMA requesters in response to the programmable mapping information.

8. Claims 2,9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heath in view of Bowes as applied to claims 1,7, and 12 above, and further in view of Solomon et al. (US Pub. No. 2004/0215868 hereinafter "Solomon").

9. Referring to apparatus claims 2 and 13, and method claim 9, the combination of Heath and Bowes teaches the system substantially as claimed, but the combination fails to teach the DMA controller comprises a crossbar.

Solomon teaches DMA controller with a crossbar (item 38 in figure 2C and paragraph 39 on page 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Heath and Bowes with the above teachings because Solomon teaches the use of this crossbar provides parallel and high bandwidth communications between devices (see lines 8-14 of paragraph 39).

10. Referring to apparatus claims 3,4, and 14, Heath discloses resolving conflicts so that each of the DMA requests is mapped to only one of the DMA channels (see paragraph bridging columns 5 and 6, note while Heath does not use the exact language of

"resolving conflicts," the arbitration system disclosed ensures that the requests are mapped to the channels on a one-to-one basis, thus resolving any conflicts).

11. Referring to claim 5, Heath discloses mapping DMA grants from the DMA channels to the respective DMA requesters (see paragraph bridging columns 5 and 6).

12. Referring to apparatus claim 6, Heath discloses mapping DMA requests and mapping DMA grants is responsive to programmable mapping information associated with each channel (see paragraph bridging columns 5 and 6, note Heath discloses that channel assignment register and priority assignment register are programmable either through the BIOS or via an application program).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following U.S. Patents are cited to further show the state of the art as it pertains to the applicant's invention:

U.S. Patent No. 6,735,639 to Higuchi teaches a DMA controller comprising a plurality of channels, each comprising a datapath and control logic; and

U.S. Patent No. 5,826,106 to Pang teaches a DMA controller transferring data according to programmable channel mapping information.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
August 29, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
8/30/06